

CONFORMAL SURFACE SILICIDE STRAP ON SPACER AND METHOD OF
MAKING SAME

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FIELD OF THE INVENTION

[0001] The present invention relates to interconnect structures in a semiconductor device. More specifically, the present invention relates to an interconnect strap located over a spacer of a semiconductor structure.

RELATED ART

[0002] Figs. 1A-1D are cross sectional views illustrating the fabrication of a conventional interconnect strap. As illustrated in Fig. 1A, gate oxide 102, gate electrodes 103-104, and silicon nitride spacers 105-108 are formed over substrate 101. Lightly doped regions 109-110 and dielectric 111 are formed in substrate 101. As illustrated in Fig. 1B, photoresist layer 112 is coated, exposed and developed, such that an opening 113 is formed through photoresist layer 112, exposing spacer 106. An etch step is then performed, thereby removing spacer 106 through opening 113. As illustrated in Fig. 1C, photoresist layer 112 is stripped, and source/drain implant steps are performed, thereby forming source/drain regions 114-115. As illustrated in Fig. 1D, self-aligned CoSi₂ is formed on source/drain regions 114-115 and gate electrodes 103-104 using high temperature sputtering and in-situ vacuum

annealing. Gate electrode 103 and source/drain region 114 are connected by CoSi_2 strap 116, which is formed where spacer 106 was removed.

[0003] Disadvantages associated with the process of Figs. 1A-1D are as follows. First, additional processing is required to selectively and completely remove spacer 106. This additional processing may present challenges depending on the composition of the spacer material and the intermediate film between spacer 106 and substrate 101, especially since photoresist layer 112 must remain in place during the removal process. Incomplete removal of spacer 106 will result in failure to form continuous CoSi_2 strap 116, because CoSi_2 will not form over remaining portions of spacer 106 (i.e., silicon nitride).

[0004] In addition, increased junction leakage will result underneath CoSi_2 strap 116 because the source/drain implant must be performed after spacer 106 is selectively removed and before the CoSi_2 is deposited. As a result, source/drain region 114 fully overlaps the lightly doped region 109 under gate electrode 103, thereby resulting in a shallow and abrupt diode junction underneath CoSi_2 strap 116.

[0005] Furthermore, CoSi_2 must be formed on a vertical sidewall of gate electrode 103. Inadequate cobalt deposition step coverage will result in failure to form a continuous CoSi_2 strap 116.

[0006] It would therefore be desirable to have a silicide strap that couples a gate electrode to a source/drain region, while overcoming the above-described shortcomings of the prior art.

SUMMARY

[0007] Accordingly, the present invention provides a method for forming a low-resistance local interconnect structure over an insulator such as a sidewall spacer dielectric. In one embodiment, the method involves fabricating a low-resistance surface strap having a relatively small area between a MOSFET polysilicon gate area and an adjacent source/drain silicon area.

[0008] A semiconductor structure is provided that includes a gate, a dielectric spacer located adjacent to a sidewall of the gate, a source/drain region, and a continuous silicide strap located over the gate, the dielectric spacer and the source/drain region. The silicide strap provides an electrical connection between the gate and the source drain region.

[0009] In one embodiment, the silicide strap is formed by a method that includes the steps of (1) implanting a semiconductor material, such as silicon, into upper surfaces of the gate, the dielectric spacer, and the source/drain region, (2) depositing a refractory metal over the implanted semiconductor material, and (3) reacting the refractory metal with the implanted semiconductor material, thereby forming the continuous silicide strap at the upper surfaces of the gate, the dielectric spacer and the source/drain region.

[0010] This method differs from the prior art, because the low resistance strap is formed on the surface of a spacer that is left intact instead of being removed by additional process steps prior to strap formation. In addition, the source/drain regions are completely formed prior to the formation of the strap,

thereby eliminating problems associated with shallow diode junctions being formed under the strap.

[0011] The present invention will be more fully understood in view of the following description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Figs. 1A-1D are cross sectional views illustrating the fabrication of a conventional interconnect strap.

[0013] Figs. 2A-2I are cross sectional views illustrating the fabrication of a silicide strap over a sidewall spacer in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0014] Fig. 2A is a cross sectional view of a CMOS structure 200, which includes p-type semiconductor substrate 201, gate dielectric layers 202-203, gate electrodes 204-205, dielectric sidewall spacers 206-209 and n-type source/drain regions 210-212. The structure of Fig. 2A is fabricated using conventional CMOS processing techniques, which are well known to one of ordinary skill in the art.

[0015] In the described embodiment, substrate 201 is p-type monocrystalline silicon, and gate dielectric layers 202-203 are thermally grown silicon oxide layers. In addition, gate electrodes 204-205 are conductively doped polycrystalline silicon. In the described embodiment, gate electrodes 204-205 have a length of about 0.18 microns. However, gate dimensions of less

than 0.18 microns can be used in other embodiments, assuming that overlay is tightly controlled. Sidewall spacers 206-209 can be either silicon nitride (Si_3N_4) or silicon oxide (SiO_2) with varying stoichiometries of the bulk film being deposited on the sidewall. In a particular embodiment, sidewall spacers 206-209 are formed from a silicon-rich oxide or nitride. Silicon rich oxide or nitride has an atomic silicon content greater than the silicon content of exactly stoichiometric SiO_2 or Si_3N_4 . As will become apparent in view of the disclosure below, a silicon-rich spacer material will promote the subsequent formation of a silicide strap over spacer 207. Source/drain regions 210-212 include lightly doped n-type regions, which extend under gate electrodes 204-205, as well as more heavily doped n-type regions which can provide contact regions for a subsequently formed interconnect structure (not shown). Advantageously, source/drain regions 210-212 are completely formed by this early step of the process.

[0016] As illustrated in Fig. 2B, a conformal insulating layer, which is hereinafter referred to as silicon blocking layer 213, is deposited over the structure of Fig. 2A. In the described embodiment, silicon-blocking layer 213 is silicon oxide or silicon nitride, having a thickness of at least 10 nm. Silicon-blocking layer 213 may be deposited using conventional PECVD (plasma enhanced CVD) at temperatures of about 400°C. LPCVD (low pressure thermal CVD) at temperatures of about 700°C may also be used. Either process may be used to deposit TEOS, SiO_2 or Si_3N_4 to a thickness

greater than 10 nm. As described in more detail below, silicon-blocking layer 213 will be used as a mask during a subsequent silicon implant step.

[0017] As illustrated in Fig. 2C, a photoresist layer 214 is coated over the upper surface of silicon blocking layer 213. Photoresist layer 214 is exposed and developed, thereby forming opening 215. As described in more detail below, opening 215 defines the location of a subsequently formed silicide strap. Fig. 2C further illustrates spacing requirements of opening 215 in accordance with one embodiment of the present invention. In the described embodiment, there must be at least 0.1 microns from the right edge of gate 204 to the left edge of opening 215. This ensures that the subsequently formed strap will properly contact gate electrode 204. In addition, there must be at least 0.15 microns from the left edge of gate electrode 205 to the right edge of opening 215. This ensures that the subsequently formed strap will not contact gate electrode 205.

[0018] As illustrated in Fig. 2D, silicon blocking layer 213 is etched through opening 215 of photoresist layer 214, thereby exposing a portion of gate electrode 204, sidewall spacer 207, and a portion of source/drain region 211. This etch can involve a chemical etch or a reactive ion etch. This etch must be selective with respect to the material present in sidewall spacer 207, thereby minimizing the loss of spacer 207 during the etch. Silicon-blocking layer 213 (silicon nitride) is removed using an anisotropic reactive ion etch (RIE) at

a pressure of about 200 mT, a power of about 180 W, and a mixture of AR/CF₄/O₂ gasses.

[0019] As illustrated in Fig. 2E, a silicon implant is performed through opening 215. This silicon implant is performed at a sufficiently high dose and low energy, thereby providing a peak silicon concentration of at least 55% near the exposed surface of dielectric spacer 207. In one embodiment, the silicon implant is performed at a dose of 7E15 ions/cm², energy of 10 KeV and a tilt angle of about 7 degrees with respect to the vertical axis in Fig. 2E (with substrate 201 being subjected to four 90° rotations about the vertical axis).

[0020] At the end of the silicon implantation, a silicon region 216 exists at the upper exposed surfaces of gate electrode 204, spacer 207 and source/drain region 211. The silicon implant therefore modifies the surface of dielectric spacer 207 such that it is possible to form silicide on the surface of spacer 207. That is, the silicon implant provides seed material for silicide formation over the spacer dielectric, thereby enabling the formation of low resistance silicide on a surface where silicide would not otherwise form. The silicon implant also serves to amorphize the exposed surfaces of gate 204 and source/drain region 211, which is beneficial for silicide formation. Although the present invention is described using a silicon implant step, it is understood that other semiconductor material, such as Germanium (Ge), can be deposited in other embodiments.

[0021] As illustrated in Fig. 2F, photoresist layer 214 is stripped and the upper surface of the resulting

structure is cleaned. In one embodiment, a wet cleaning process is used wherein the structure is immersed in, or sprayed with, dilute aqueous HF acid at 25°C. The HF dilution is between 1% and 10% in one embodiment.

[0022] In an alternate embodiment, the silicon implant step can be performed after photoresist layer 214 is stripped. In this case, silicon-blocking layer 213 is used as an implant hardmask to prevent the implantation of silicon outside of the area exposed by opening 215. In this embodiment, silicon-blocking layer 213 must have a thickness of at least 100 nm.

[0023] As illustrated in Fig. 2G, a refractory metal layer 217 is deposited over the resulting structure. In the described embodiment, refractory metal layer 217 includes cobalt (Co) and titanium nitride (TiN), and has a thickness of 10 nm or greater, depending on the step coverage. In one embodiment, Co is deposited first with a thickness between 5 nm and 20 nm using PVD processing. Process temperatures should be maintained between 0 and 200°C. Without breaking vacuum in the deposition chamber, TiN is deposited over the Co to a thickness of 15 to 30 nm using PVD processing. In other embodiments, TiN may not be necessary to cover the reactive metal (i.e., Co). The step coverage of sidewall spacer 207 should be maximized to increase the eventual silicide thickness on sidewall spacer 207. In other embodiments, other refractory metals, such as titanium or nickel can be used in place of cobalt. Note that the TiN layer is not required when titanium is used in place of cobalt.

[0024] As illustrated in Fig. 2H, an anneal is performed, thereby causing the refractory metal layer to

react with underlying silicon region 216 to form silicide (i.e., CoSi_x) strap 218. In one embodiment, a high temperature anneal (i.e., temperature $> 800^\circ\text{C}$), is performed to promote Co/Si creep. Co/Si creep refers to the diffusion of silicon atoms into the cobalt film. Increased Co/Si creep increases the thickness of a CoSi_2 strap which is formed during the anneal, thereby reducing the final resistance of the strap. As mentioned above, if spacer 207 is originally fabricated from a silicon-rich dielectric material, the silicide formation will be promoted during this step.

[0025] As illustrated in Fig. 2I, a selective etch is performed after the anneal step, thereby removing the un-reacted portions of refractory metal layer 217. In one embodiment, the selective etch is performed using an SPM Piranha ($\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$) and SC-1 ($\text{DI}/\text{H}_2\text{O}_2/\text{NH}_4/\text{OH}$ 5:1:05) solution. After this selective etch is performed, metal silicide strap 218 remains over the upper surface of gate electrode, sidewall spacer 207 and source/drain region 211. Silicide strap 218 provides a low-resistance connection between gate electrode 204 and source/drain region 211.

[0026] Processing can then continue using conventional CMOS processing techniques.

[0027] Note that compared to a conventional CMOS process flow, the present invention requires the deposition of an additional dielectric film in order to form silicon block layer 213 and the processing of one additional photoresist layer 214. The present invention can therefore be easily integrated into a conventional

CMOS process. The present invention is therefore a low cost and readily manufacturable technology feature.

[0028] Although the invention has been described in connection with several embodiments, it is understood that this invention is not limited to the embodiments disclosed, but is capable of various modifications that would be apparent to a person skilled in the art. For example, although the described examples describe the formation of a silicide strap from a gate to a source/drain region, it is understood that the silicide strap can provide connections to other structures over a dielectric spacer. Thus, the invention is limited only by the following claims.